

Verification of Spectre Mitigations using Hypersimulations

Jonathan Baumann

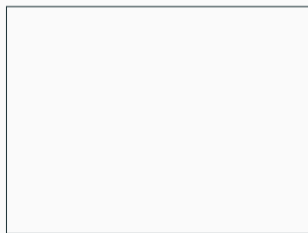
August 09, 2023

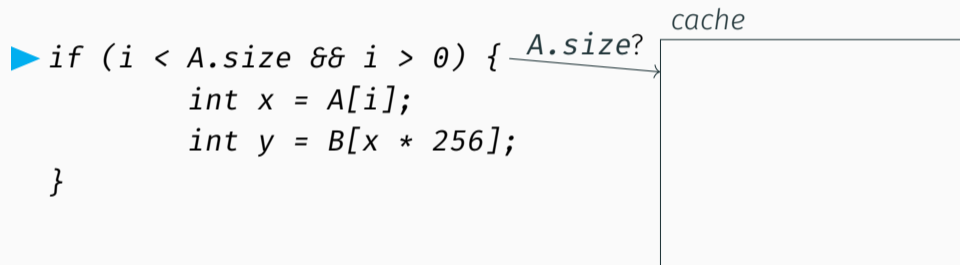


UNIVERSITÄT
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SAARLANDES

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    int x = A[i];  
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}
```

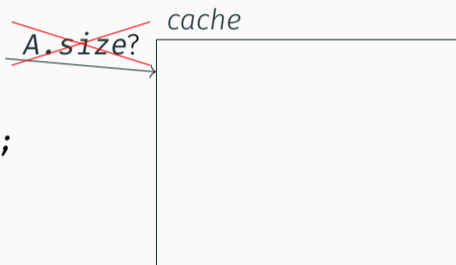
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~~A.size?~~ cache



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Spectre Mitigations

- Hardware Mitigations

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 - ⇒ costly, can only protect future hardware

Spectre Mitigations

- Hardware Mitigations
- Software mitigations

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- Software mitigations
 - Program Analysis and Repair

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 - SPECTECTOR: symbolic execution

Spectre Mitigations

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 - Compiler Countermeasures

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 - Intel: Fence instructions after branches
 - Speculative Load Hardening: additional data dependencies
 - MSVC: Fence instructions, pattern-based

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- Design and verify a mitigation that could not be verified previously

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- Method of verifying compiler-based spectre mitigations
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- Verify Intel's mitigation for three leakage models
- Incompatibility between speculative load hardening and always-mispredict semantics
- Design and verify a mitigation that could not be verified previously
- All work formalized in the Coq Proof Assistant

Noninterference

Same public inputs \implies Same observations

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Speculative Noninterference

Same observations
under nonspeculative
execution \implies Same observations
under speculative
execution

Applying a mitigation: Compilation



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Language without
speculative execution \longrightarrow Language with
speculative execution

- Without speculation, speculative noninterference is always satisfied

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Applying a mitigation: Compilation

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- Approximate using speculative safety

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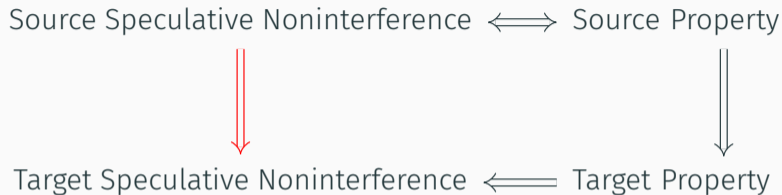
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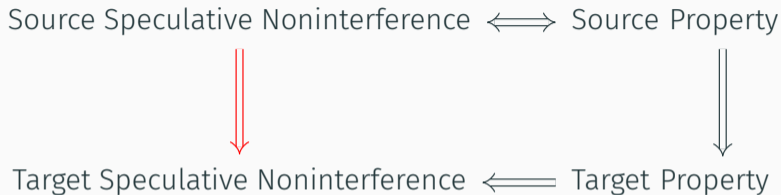
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- **Our approach does not have these limitations**

Verifying Spectre Mitigations: Preservation of Leakage Equivalence



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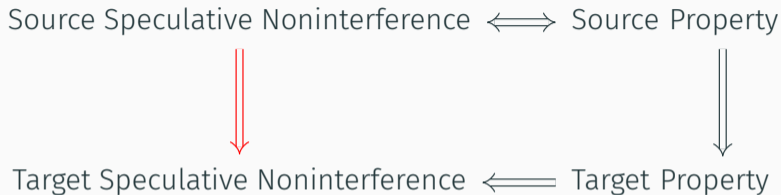
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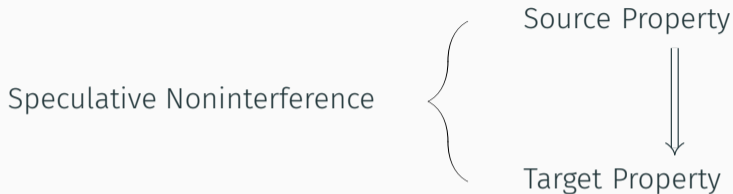
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Verifying Spectre Mitigations: Preservation of Leakage Equivalence



Speculative Noninterference

Leakage equivalence
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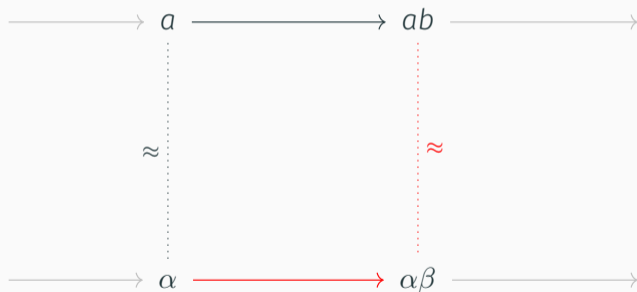
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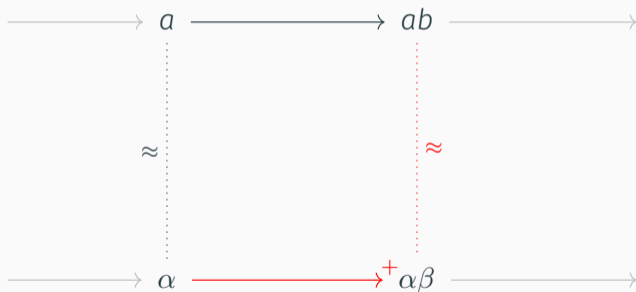
Leakage Equivalence
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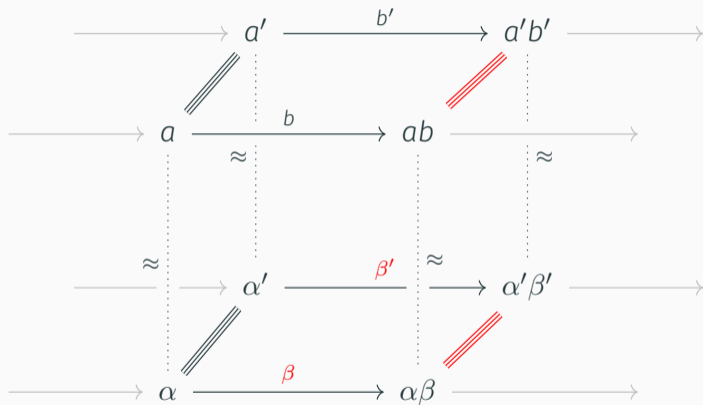
Preservation of Hyperproperties: Constant-Time Simulations [Barthe et al., 2018]



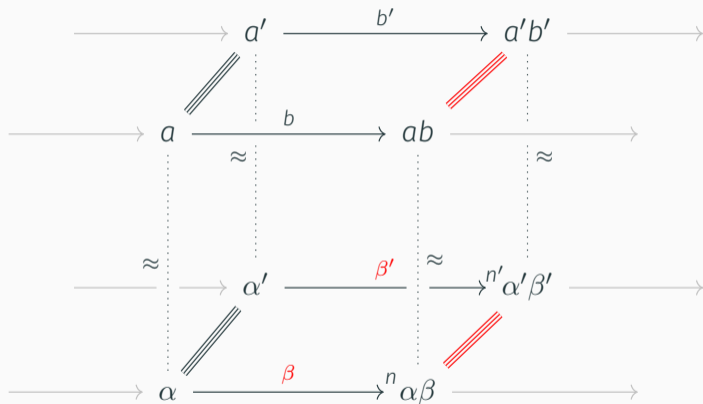
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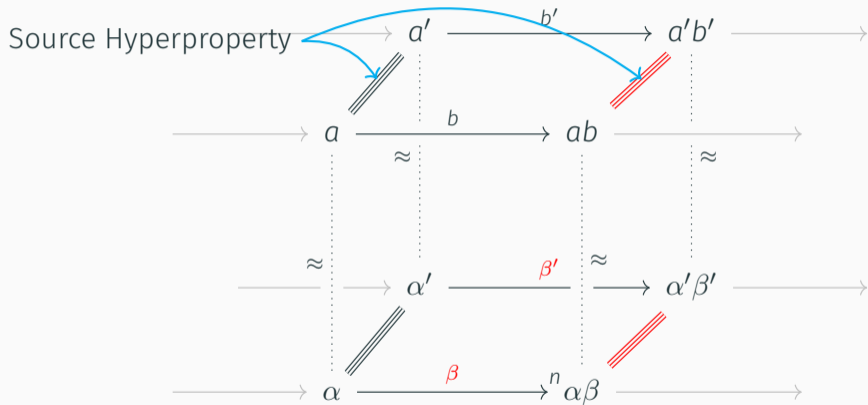
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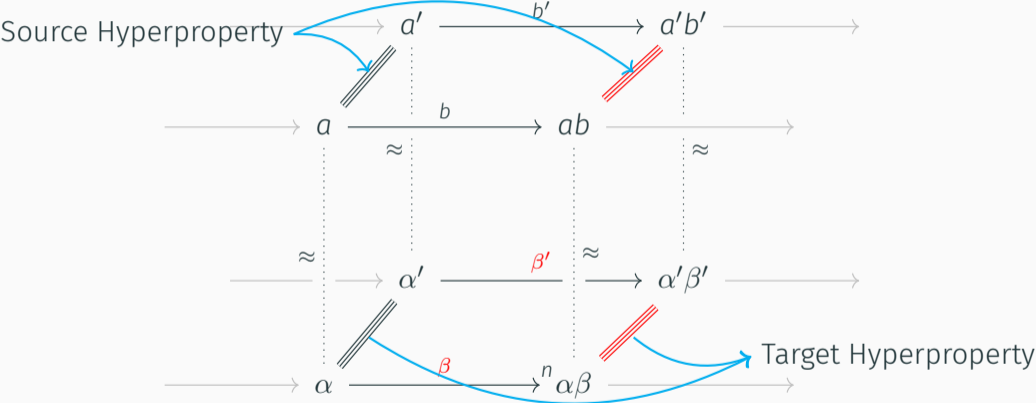
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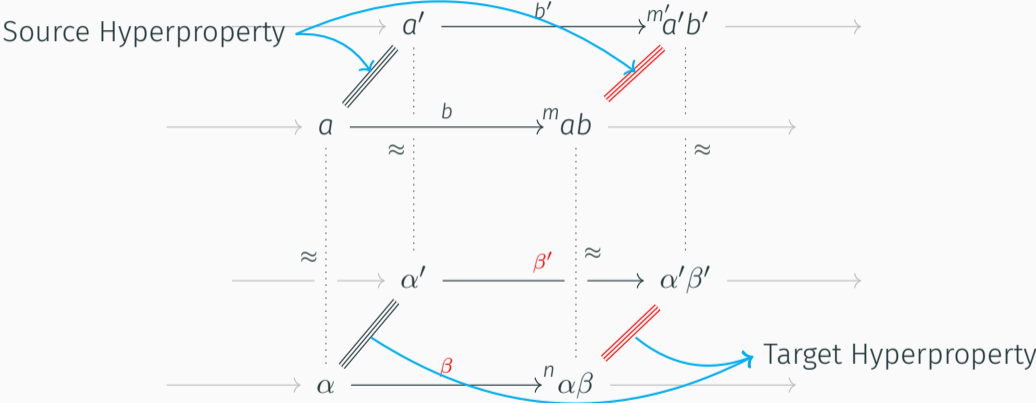
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Preservation of Hyperproperties: Hyper-Simulations [Rosemann, 2023]



Leakage Equivalence as a Property of Trace Prefixes

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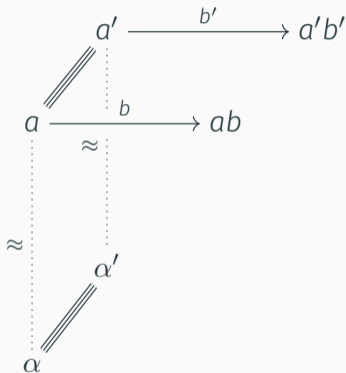


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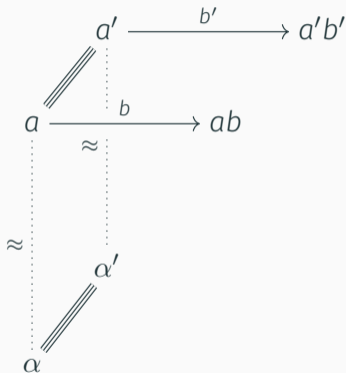
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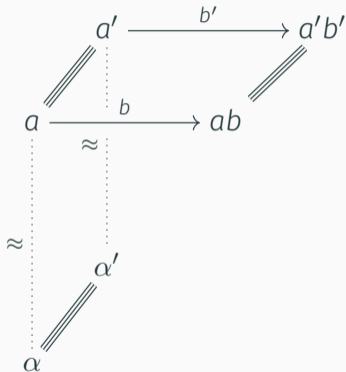
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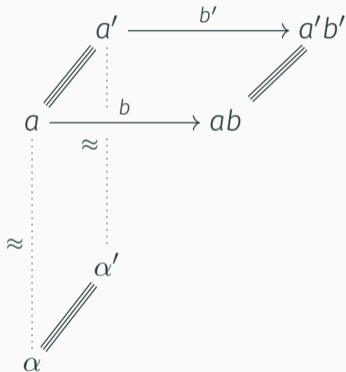
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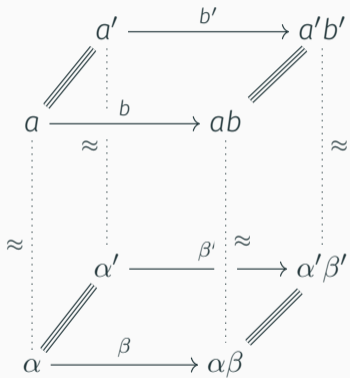
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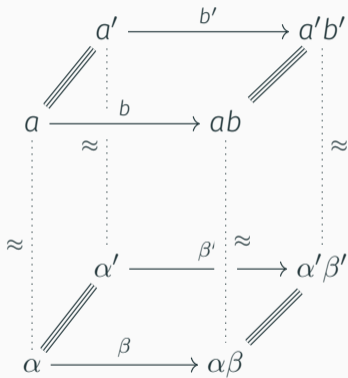
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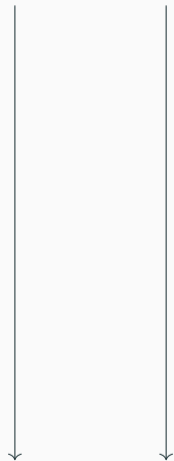
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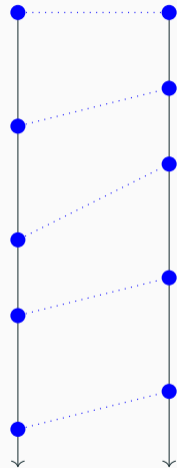
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- Prove that target relation is satisfied after hyper-step
- Conclude that target traces are leakage equivalent

Proving Preservation of Leakage Equivalence



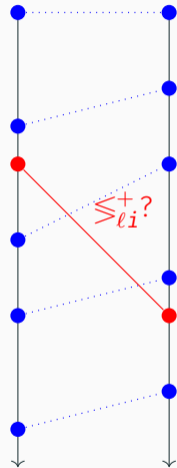
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- From hypersimulation: target relation *always holds at some future point*



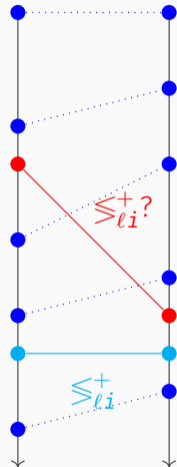
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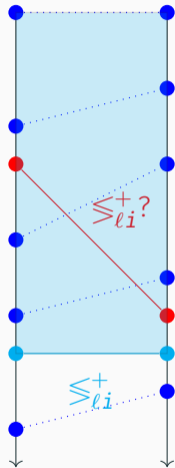
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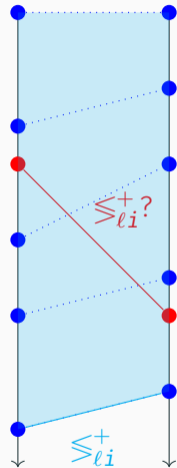
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- \leq_{li}^+ must be satisfied *at every point during execution*
- Leakage equivalence is a safety hyperproperty
 - \leq_{li}^+ satisfied at some point
 \implies satisfied at all prior points
- Target relation implies \leq_{li}^+
 $\implies \leq_{li}^+$ must hold everywhere



Modelling Speculative Execution: Toy Language

$Expr \ni e ::= n \quad n \in \mathbb{N}$
| x x is a variable name
| $e_1 + e_2$ | $e_1 - e_2$ | $e_1 \times e_2$ | $e_1 < e_2$ | $e_1 = e_2$ | $!e$

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$Stmt \ni s ::= skip$ | $x := e$
| $fence$ | $if\ e\ then\ p_1\ else\ p_2\ end$
| $read\ [e]\ x$ | $while\ e\ do\ p_1\ finally\ p_2\ end$
| $write\ [e]\ x$

- Note: we translate *while* to *if*

Modelling Speculative Execution: Speculative Semantics

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- Stack of states to allow rollback
- Speculation window determines how long to follow mispredicted paths
- Always-Mispredict semantics [Guarnieri et al., 2018] captures all possible combinations of branch predictions


```

    if x > 0
    then if x < 10
         then read [x] y
         else fence
         end
    else skip
    end

```

⟨ \perp | $[x \mapsto -1]$ | $[-1 \mapsto 42]$ |

Modelling Speculative Execution: Speculative Semantics

$$\frac{\text{no-rollback}(n) \quad \llbracket b \rrbracket_{\mathcal{V}} = 0}{\langle n \mid \mathcal{V} \mid \mathcal{H} \mid \text{if } b \text{ then } p_1 \text{ else } p_2 \text{ end}; p \rangle :: S} \text{AMIFFALSE}$$
$$\rightarrow_{\text{sp}} \langle \text{wndw}(n) \mid \mathcal{V} \mid \mathcal{H} \mid p_1 * p \rangle :: \langle \text{decr}(n) \mid \mathcal{V} \mid \mathcal{H} \mid p_2 * p \rangle :: S$$

$\left\langle \perp \mid [x \mapsto -1] \mid [-1 \mapsto 42] \mid \right.$

if $x > 0$
then *if* $x < 10$
 then *read* $[x] y$
 else *fence*
 end
else *skip*
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$\left. \right\rangle$

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```
⟨ 16 | [x ↦ -1] | [-1 ↦ 42] | if x < 10
  then read [x] y
  else fence end ⟩
```

```
⟨ ⊥ | [x ↦ -1] | [-1 ↦ 42] | skip ⟩
```

Modelling Speculative Execution: Speculative Semantics

```
if  $x > 0$   
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    then read  $[x]$   $y$   
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```

$\langle 15 \mid [x \mapsto -1] \mid [-1 \mapsto 42] \mid \textit{read } [x] y \rangle$

$\langle 15 \mid [x \mapsto -1] \mid [-1 \mapsto 42] \mid \textit{fence} \rangle$

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$\langle 14 \mid [x \mapsto -1, y \mapsto 42] \mid [-1 \mapsto 42] \mid \square \rangle$

$\langle 15 \mid [x \mapsto -1] \mid [-1 \mapsto 42] \mid \mathit{fence} \rangle$

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$\langle 0 \mid [x \mapsto -1] \mid [-1 \mapsto 42] \mid [] \rangle$

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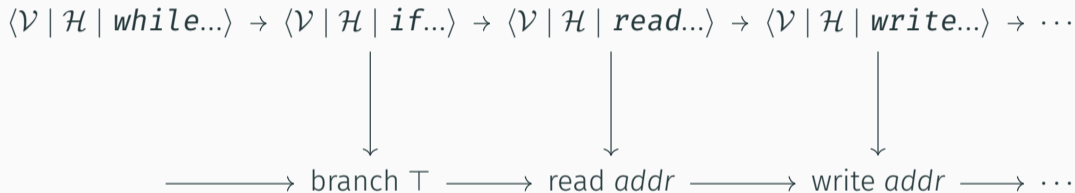
$\langle \perp \mid [x \mapsto -1] \mid [-1 \mapsto 42] \mid [] \rangle$

Modelling Side-Channel Vulnerabilities: Leakage Models

Leakage models: functions from sequences of states to sequences of observations

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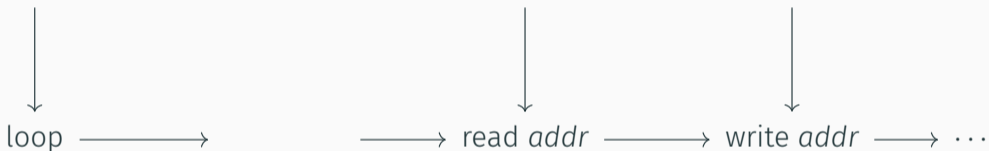
Leakage models: functions from sequences of states to sequences of observations



ℓ_{ct} control flow, memory accesses

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$$\langle \mathcal{V} \mid \mathcal{H} \mid \mathit{while}\dots \rangle \rightarrow \langle \mathcal{V} \mid \mathcal{H} \mid \mathit{if}\dots \rangle \rightarrow \langle \mathcal{V} \mid \mathcal{H} \mid \mathit{read}\dots \rangle \rightarrow \langle \mathcal{V} \mid \mathcal{H} \mid \mathit{write}\dots \rangle \rightarrow \dots$$


l_{ct} control flow, memory accesses

l_{lm} loop headers, memory accesses

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ℓ_{ct} control flow, memory accesses

ℓ_{lm} loop headers, memory accesses

ℓ_{mem} only memory accesses

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Mitigation proposed by Intel [Intel, 2018, 2021]:
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$$\langle \text{while } b \text{ do } p_1 \text{ finally } p_2 \text{ end}; p \rangle_{\text{fence}} = \text{while } b \text{ do fence; } \langle p_1 \rangle_{\text{fence}} \\ \text{finally fence; } \langle p_2 \rangle_{\text{fence}} \text{ end; } \langle p \rangle_{\text{fence}}$$

$$\langle s; p \rangle_{\text{fence}} = s; \langle p \rangle_{\text{fence}} \quad \text{otherwise}$$

$$\langle [] \rangle_{\text{fence}} = []$$

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(new result)

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ℓ_{lm} Leakage model including loop headers, but not all control flow
(*new result*)

ℓ_{mem} Leakage model without any control flow
(*new result*)

Issues with Speculative Load Hardening

Speculative Load Hardening [Carruth, 2018]:

Protect memory access with artificial data dependencies

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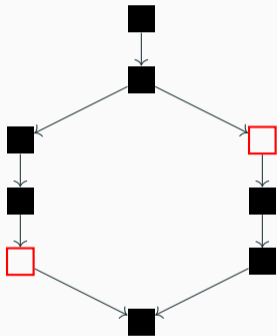
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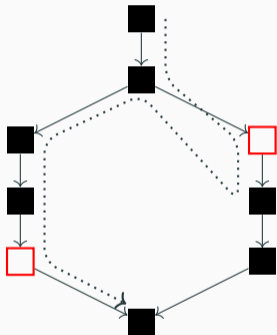
Protect memory access with artificial data dependencies

- Special register accumulates path conditions
 - data dependency on branch conditions
 - detects speculative execution
- Memory accesses compute address using special register
 - original address during nonspeculative execution
 - known safe address during speculative execution

Issues with Speculative Load Hardening



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- More accurate semantics *with vendor guarantees* needed

read [1] x; if $x \geq 0$ then read [x] y else read [x] y end; write [1] y

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Relaxed insertion of fences:

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Relaxed insertion of fences:

- At every branch, check the sequence of *read* and *write* instructions
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- Proof-of-concept implementation has some additional restrictions

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 - Restrictions can be lifted with future work
- ⇒ reasonable mitigations that were not covered before

Patrignani and Guarnieri [2021] support

Further Work

Patrignani and Guarnieri [2021] support

- function calls

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Other applications:

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- more precise semantics based on hardware guarantees

Our approach

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- enables reasoning about more leakage models
 - control flow does not need to be included
- verifies mitigations that could not be verified before
 - such mitigations are reasonable, not contrived examples

- Gilles Barthe, Benjamin Grégoire, and Vincent Laporte. Secure compilation of side-channel countermeasures: The case of cryptographic “constant-time”. In *31st IEEE Computer Security Foundations Symposium, CSF 2018, Oxford, United Kingdom, July 9-12, 2018*, pages 328–343. IEEE Computer Society, 2018. doi: 10.1109/CSF.2018.00031. URL <https://doi.org/10.1109/CSF.2018.00031>.
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- Marco Patrignani and Marco Guarnieri. Exorcising spectres with secure compilers. In Yongdae Kim, Jong Kim, Giovanni Vigna, and Elaine Shi, editors, *CCS '21: 2021 ACM SIGSAC Conference on Computer and Communications Security, Virtual Event, Republic of Korea, November 15 - 19, 2021*, pages 445–461. ACM, 2021. doi: 10.1145/3460120.3484534. URL <https://doi.org/10.1145/3460120.3484534>.
- Julian Rosemann. Private communications, not yet released. All relevant proofs are included in the Coq development, 2023.

$$\frac{}{\langle \mathcal{V} \mid \mathcal{H} \mid \mathit{skip}; p \rangle \rightarrow_{\text{ns}} \langle \mathcal{V} \mid \mathcal{H} \mid p \rangle} \text{SKIP} \qquad \frac{}{\langle \mathcal{V} \mid \mathcal{H} \mid \mathit{fence}; p \rangle \rightarrow_{\text{ns}} \langle \mathcal{V} \mid \mathcal{H} \mid p \rangle} \text{FENCE}$$

$$\frac{[[e]]_{\mathcal{V}} = v}{\langle \mathcal{V} \mid \mathcal{H} \mid x := e; p \rangle \rightarrow_{\text{ns}} \langle \mathcal{V}[x \mapsto v] \mid \mathcal{H} \mid p \rangle} \text{ASSIGN}$$

$$\frac{[[a]]_{\mathcal{V}} = a' \quad \mathcal{H}(a') = v}{\langle \mathcal{V} \mid \mathcal{H} \mid \mathit{read} [a] x; p \rangle \rightarrow_{\text{ns}} \langle \mathcal{V}[x \mapsto v] \mid \mathcal{H} \mid p \rangle} \text{READ}$$

$$\frac{[[a]]_{\mathcal{V}} = a' \quad \mathcal{V}(x) = v}{\langle \mathcal{V} \mid \mathcal{H} \mid \mathit{write} [a] x; p \rangle \rightarrow_{\text{ns}} \langle \mathcal{V} \mid \mathcal{H}[a' \mapsto v] \mid p \rangle} \text{WRITE}$$

$$\frac{\llbracket b \rrbracket_{\mathcal{V}} \neq 0}{\langle \mathcal{V} \mid \mathcal{H} \mid \text{if } b \text{ then } p_1 \text{ else } p_2 \text{ end}; p \rangle \rightarrow_{\text{ns}} \langle \mathcal{V} \mid \mathcal{H} \mid p_1 \# p \rangle} \text{IFTRUE}$$

$$\frac{\llbracket b \rrbracket_{\mathcal{V}} = 0}{\langle \mathcal{V} \mid \mathcal{H} \mid \text{if } b \text{ then } p_1 \text{ else } p_2 \text{ end}; p \rangle \rightarrow_{\text{ns}} \langle \mathcal{V} \mid \mathcal{H} \mid p_2 \# p \rangle} \text{IFFALSE}$$

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$$\frac{}{\langle \mathcal{V} \mid \mathcal{H} \mid [] \rangle \rightarrow_{\text{ns}} \langle \mathcal{V} \mid \mathcal{H} \mid [] \rangle} \text{TERM}$$

$$\text{decr}(n) := \begin{cases} \perp & \text{if } n = \perp \\ n - 1 & \text{otherwise} \end{cases}$$

$$\text{wndw}(n) := \begin{cases} \omega & \text{if } n = \perp \\ n - 1 & \text{otherwise} \end{cases}$$

$$\text{no-rollback}(n) := n > 0 \vee n = \perp$$

$$\text{zero-out}(n) := \begin{cases} \perp & \text{if } n = \perp \\ 0 & \text{otherwise} \end{cases}$$

$$\frac{\text{no-rollback}(n)}{\langle n \mid \mathcal{V} \mid \mathcal{H} \mid \mathbf{skip}; p \rangle :: S \rightarrow_{\text{sp}} \langle \text{decr}(n) \mid \mathcal{V} \mid \mathcal{H} \mid p \rangle :: S} \text{AMSKIP}$$

$$\frac{\text{no-rollback}(n)}{\langle n \mid \mathcal{V} \mid \mathcal{H} \mid \mathbf{fence}; p \rangle :: S \rightarrow_{\text{sp}} \langle \text{zero-out}(n) \mid \mathcal{V} \mid \mathcal{H} \mid p \rangle :: S} \text{AMFENCE}$$

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$$\frac{\text{no-rollback}(n) \quad \llbracket a \rrbracket_{\mathcal{V}} = a' \quad \mathcal{V}(x) = v}{\langle n \mid \mathcal{V} \mid \mathcal{H} \mid \mathbf{write} [a] x; p \rangle :: S \rightarrow_{\text{sp}} \langle \text{decr}(n) \mid \mathcal{V} \mid \mathcal{H}[a' \mapsto v] \mid p \rangle :: S} \text{AMWRITE}$$

$$\frac{\text{no-rollback}(n)}{\rightarrow_{\text{sp}} \langle n \mid \mathcal{V} \mid \mathcal{H} \mid \mathit{while} \ e \ \mathit{do} \ p_1 \ \mathit{finally} \ p_2 \ \mathit{end}; \rangle :: S} \quad \text{AMWHILE}$$

$$\langle \text{decr}(n) \mid \mathcal{V} \mid \mathcal{H} \mid \mathit{if} \ e \ \mathit{then} \ (p_1 \# [\mathit{while} \ e \ \mathit{do} \ p_1 \ \mathit{finally} \ p_2 \ \mathit{end}]) \ \mathit{else} \ p_2 \ \mathit{end}; p \rangle :: S$$

$$\frac{\text{no-rollback}(n) \quad \llbracket b \rrbracket_{\mathcal{V}} \neq 0}{\rightarrow_{\text{sp}} \langle n \mid \mathcal{V} \mid \mathcal{H} \mid \mathit{if} \ b \ \mathit{then} \ p_1 \ \mathit{else} \ p_2 \ \mathit{end}; p \rangle :: S} \quad \text{AMIFTRUE}$$

$$\rightarrow_{\text{sp}} \langle \text{wndw}(n) \mid \mathcal{V} \mid \mathcal{H} \mid p_2 \# p \rangle :: \langle \text{decr}(n) \mid \mathcal{V} \mid \mathcal{H} \mid p_1 \# p \rangle :: S$$

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$$\frac{}{\langle 0 \mid \mathcal{V} \mid \mathcal{H} \mid p \rangle :: S \rightarrow_{\text{sp}} S} \text{AMROLLBACK}$$

$$\frac{n \neq \perp \wedge n > 0}{\langle n \mid \mathcal{V} \mid \mathcal{H} \mid [] \rangle :: S \rightarrow_{\text{sp}} S} \text{AMROLLBACKT}$$

$$\frac{}{\langle \perp \mid \mathcal{V} \mid \mathcal{H} \mid [] \rangle :: S \rightarrow_{\text{sp}} \langle \perp \mid \mathcal{V} \mid \mathcal{H} \mid [] \rangle :: S} \text{AMTERM}$$

$$\frac{}{[] \rightarrow_{\text{sp}} []} \text{AMTERM}'$$

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Speculative safety implies speculative noninterference

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- **Our approach does not have these limitations**

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